Amendments To The Specification

Please amend the specification by making the following amendments:

Please substitute the following for the first full paragraph on Page 4:

Referring to FIGURE 1 of the drawings, the reference numeral 100 generally designates a phase-locked loop (PLL) along with a test apparatus to characterize a voltage-controlled oscillator (VCO). The PLL 100 comprises first and second delays RXs 102 and 104, a phase-frequency detector (PFD) 108, a first and second frequency dividers 110 and 112, a charge pump (CP) 114, a loop filter ~~(LP)~~ (LF) 116, a reference current generator IREF 118, a voltage-controlled oscillator (VCO) 120, a divider clock enable unit 122, a third frequency divider 124, and a first multiplexer 126.

Please substitute the following for the second full paragraph on Page 4:

The first delay RX 102 is coupled to the PFD 108. The PFD 108 is coupled to the CP 114 for providing UP and DN signals to the CP 114. The CP 114 is also coupled to the LF 116, which in this implementation includes a ~~CFILT~~ CFLT capacitance. The LF 116 is also coupled to the VCO 120 to provide an input voltage CNTL to the VCO 120. Optionally, the output of the PFD 108 is also coupled to a feedforward input FF of the VCO 120. The reference current generator IREF 118 is also coupled to both the CP 114 and the VCO 120. The PFD 108 is also coupled to the second frequency divider 112, which is coupled to the first frequency divider 110. Specifically, the first frequency divider 110 is a pre-scaler, and the second frequency divider 112 is a programmable

frequency divider. The first frequency divider 110 is also coupled to the second delay RX 104 to receive PLL_OUT signal.

Please substitute the following for the first full paragraph on Page 5:

The first multiplexer 126 is coupled to the VCO 120 both directly and through the divider clock enable unit 122 and the third frequency divider 124. The first multiplexer 126 also receives a fixed-level voltage VFB. A select signal VCOMUX selects one of these three inputs as a PLL clock signal PLL_OUT ~~one of these three inputs~~. The PLL_OUT [[fed]] feeds back to the second delay RX 104.

Please substitute the following for the second full paragraph on Page 8:

Now referring to FIGURE 10, a schematic diagram 1000 illustrates a PLL along with a test apparatus to further characterize a VCO. The schematic diagram 1000 largely includes a PLL 1002 and a test apparatus 1004 coupled to the PLL 1002. The PLL 1002 generally includes a PFD 1006, a CP and [[LP]] LF 1008, a VCO 1010, and a frequency divider 1012. The configuration of various elements of the PLL 1002 is well known in the art, and may be modified without departing from the true spirit of the present invention. Preferably, the test apparatus 1004 includes N resistors coupled in series between supply voltage V_{DD} and ground, N+1 transmission gates TG0 through TGN, and a test scan signal generator 1014, where N is an integer greater than or equal to 1. Note that all transmission gates function basically as low-impedance switches and thus may be replaced with other devices with similar switch functionality.

Please substitute the following for the third full paragraph on Page 11:

In FIGURE 13, a timing diagram 1300 illustrates a VCO frequency ~~CLK_Out~~ CLK_OUT for a particular VCO input voltage V_C under certain bias conditions of FIGURE 12. When the pad 1206 is coupled to GND and the transmission gate TGV is turned on, the schematic diagram 1200 becomes very similar to the schematic diagram 1000, except that a voltage drop across the transmission gate TGV when TGV is turned on may have to be taken into account. Hence, the following equation for the VCO input voltage V_C in a test mode: